ABSTRACT OF THE DISCLOSURE

A bi-directional serializer/de-serializer is disclosed using a single bi-directional data line and a single bi-directional clock line. Gated buffers are controlled to operate either sending or receiving data, and a phase locked loop provides a clock to shift data out from a shift register. A reference clock is supplied to the PLL and the PLL generates a synchronous bit clock. The bit clock is sent over the clock line in parallel with the serial data bits, and the PLL bit clock is synchronized to the data bits. The receiving system will use the bit clock to serial load a receiving shift register. When a word is received a word clock is available to inform the receiving system. An embodiment of the system sends data to a receiving system using a clock generated at the sending system. Another embodiment receives data but uses a clock that is sent from the receiving system to the sending system, wherein the sending system uses the received clock to generate a clock to send the data and a synchronous clock that is sent back to the receiving system to load the data from the data line.